Predictive Power Control for T-Type Nested Neutral Point Clamped Inverter Without Weighting Factor and Reduced Computational Burden

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Abstract—This paper offers a simplified method for direct power control employing model predictive control (MPC) for a four-level T-type Nested Neutral Point Clamped inverterconnected grid. A discrete-time model is used to forecast the grid current and power for evaluating the cost function. Unlike the traditional MPC, which utilizes exhaustive searches for all viable switching combinations, the proposed method only considers the possible candidates based on the needed inverter voltage sector for the optimization loop during the initial stage. During the second phase, the redundant switching status, which is considered the best output vector, will be employed to balance the capacitor voltages. Therefore, the computation load is not only dramatically reduced but also eliminated the weighting factors tuning by the suggested approach. The proposed method's efficacy is substantiated through comparative simulation studies conducted under both steady-state and dynamic-state operations.

Index Terms—T-type Nested Neutral Point Clamped inverter, Model predictive control, Direct power control, Capacitor voltage balancing, Computational burden.

I. INTRODUCTION

A multilevel inverter is considered a reasonable solution for high power at medium voltage thanks to its benefits: lower harmonic inverter voltage, voltage stress of the switches, and increased power capacity [1]–[3]. Compared with the fourlevel inverters, the T-type four-level Nested Neutral Point Clamped (4L-T-type NNPC) inverter exhibits many outstanding characteristics, including an extensive voltage range without series connected switches and a decreased number of elements [4]–[6]. Therefore, this configuration is appropriate for different high-power electric applications for example renewable energy conversion systems, transmission systems, and medium voltage motor drives.

The linear controllers are widely used for controlling the inverters. However, low transient performance and precise

parameters of PI controllers are the limitations of this method. Another disadvantage of this method is a complicated modulation technique to balance the voltages of the flying capacitors [1], [7]. The direct power control technique, introduced recently for enhanced control performance [1], utilizes a hysteresis approach and a lookup table determined by the error between desired and estimated values of grid powers. Despite achieving rapid transient response, the disadvantages of this method include significant grid power ripples, as well as a high sampling frequency. Nowadays, the finite control set model predictive control (FCS-MPC) has demonstrated as a remarkable and efficient technique for electrical applications thanks to the simple control structure and easy implementation [1], [3], [8]. A notable advantage of FCS-MPC lies in its ability to incorporate the nonlinearities of multiple-input multipleoutput systems, further restrictions, and compensate for system delays.

This paper presents a simplified strategy for direct power control that utilizes FCS-MPC to regulate a grid connected to a four-level T-Type Nested Neutral Point Clamped Inverter. A dynamic representative is utilized to anticipate the grid current and power performance, enabling the assessment of the cost function. In contrast to the standard FCS-MPC, which evaluates all switching sequences of the inverters, the proposed strategy only assesses the feasible candidates based on the position of the desired inverter voltage in the initial stage. The redundant switching status, which is taken into account as the best inverter output voltage, is applied to ensure the balance of flying capacitor voltages in the second stage. Consequently, the calculation time is not only significantly diminished but also eliminated the weighting factors selection. The efficiency of the suggested approach is validated by relative simulation investigation under steady-state and transient-state.

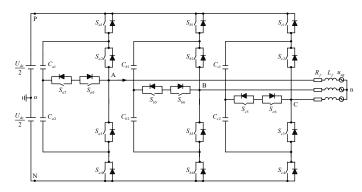


Fig. 1: Topology of the grid-tie 4L-T-type NNPC inverter.

II. DYNAMIC MODEL OF T-TYPE NNPC INVERTER

Fig. 1 illustrates a facilitated configuration of the grid-tie 4L-T-type NNPC inverter [2]. This structure is an integration of a flying capacitor and a T-type configuration that provides a four-level inverter voltage by keeping all flying capacitor (FC) voltages at one out of every three parts of overall DC bus voltage. The four output voltage levels are $-U_{dc}/2$, $-U_{dc}/6$, $U_{dc}/6$ and $U_{dc}/2$ which correspond to six feasible switching states 0, 1C, 1D, 2C, 2D and 3. Switching states 3 and 0 don't impact on the flying capacitor voltage, whereas, four states 1C, 1D, 2C, and 2D have an opposite influence on the voltage of the FC in relation to the polarity of the grid current. The switching devices of each inverter leg operate in a complementary mode (S_{x1}, S_{x4}) , (S_{x2}, S_{a6}) , and (S_{a3}, S_{a6}) S_{a5}) with $x \in \{a, b, c\}$. Thus, the 4L-T-type NNPC inverters provide 216 various combinations of switching status. Table I provides an overview of the switching state in respect of output level and voltage vector for 4L-Type-NNPC inverters.

 TABLE I: The different switching status and related vectors of 4L-T-type NNPC inverter

Switching vector	Output level	Swite	ching s	tate of each leg	Voltage vector
S_x	L_x	$\overline{S_{x1}}$	S_{x2}	S_{x3}	u_{xo}
3	3	1	1	0	$U_{dc}/2$
2C	2	0	1	0	$U_{dc}/6$
2D	2	1	0	0	$U_{dc}/6$
1C	1	0	0	0	$-U_{dc}/6$
1D	1	1	0	1	$-U_{dc}/6$
0	0	0	0	1	$-U_{dc}/2$

The inverter's output voltage, calculated between the inverter terminal (x) and the midpoint of the DC-bus voltage (o), can be phrased as:

$$u_{xo} = \frac{2(L_x - 3)U_{dc}}{6},\tag{1}$$

where U_{dc} , L_x represent the voltage of DC-bus and the inverter voltage level.

The dynamic behavior of grid-side inverters is given by:

$$u_{ao} = u_{ag} + R_f i_{ag} + L_f \frac{di_{ag}}{dt} + u_{no},$$

$$u_{bo} = u_{bg} + R_f i_{bg} + L_f \frac{di_{bg}}{dt} + u_{no},$$

$$u_{co} = u_{cg} + R_f i_{cg} + L_f \frac{di_{cg}}{dt} + u_{no},$$
(2)

where u_{ag} , u_{bg} , u_{cg} , i_{ag} , i_{bg} , i_{cg} denote the grid voltage and grid current. u_{ao} , u_{bo} , and u_{co} are the three-phase inverter output voltages. The resistance and inductance of the filter are denoted as R_f and L_f , respectively. The comm-mode voltage u_{no} , expressed as the voltage between the neutral grid and the center of the DC-bus by the following equation:

$$u_{no} = \frac{1}{3} \left(u_{ao} + u_{bo} + u_{co} \right).$$
(3)

The continuous-time representation of grid current is derived according to (2) and (3):

$$\frac{di_g}{dt} = \frac{1}{L_f} \left(u_{xo} - \frac{N}{3} u_{xo} - u_{xg} \right) - \frac{R_f}{L_f} i_{xg}, \qquad (4)$$

where

$$u_{xo} = \begin{bmatrix} u_{ao} \\ u_{bo} \\ u_{co} \end{bmatrix}, u_{xg} = \begin{bmatrix} u_{ag} \\ u_{bg} \\ u_{cg} \end{bmatrix}, i_g = \begin{bmatrix} i_{ag} \\ i_{bg} \\ i_{cg} \end{bmatrix}, \quad (5)$$

N is 3x3 one matrix.

The discrete-time formulation of the grid current is achieved from (5) through the utilization of the forward Euler approach:

$$i_{g}(k+1) = i_{g}(k) \left(1 - \frac{T_{s}R_{f}}{L_{f}}\right)$$

$$+ \frac{T_{s}}{L_{f}} \left(u_{xo}(k) - \frac{N}{3}u_{xo}(k) - u_{xg}(k)\right),$$
(6)

where T_s stand for the sampling period.

The dynamic behavior of grid active power and reactive power is calculated by the elements of grid voltage and current in the stationary reference frame [7]:

$$P_{g} = \frac{3}{2} \left(u_{g\alpha} i_{g\alpha} + u_{g\beta} i_{g\beta} \right), \tag{7}$$
$$Q_{g} = \frac{3}{2} \left(u_{g\beta} i_{g\alpha} - u_{g\alpha} i_{g\beta} \right).$$

where $u_{g\alpha}$, $u_{g\beta}$, $i_{g\alpha}$ and $i_{g\beta}$ can be achieved from the $\alpha\beta$ transformation:

$$\begin{bmatrix} u_{g\alpha} \\ u_{g\beta} \end{bmatrix} = \begin{bmatrix} C \end{bmatrix} \begin{bmatrix} u_{ag} \\ u_{bg} \\ u_{cg} \end{bmatrix}, \begin{bmatrix} i_{g\alpha} \\ i_{g\beta} \end{bmatrix} = \begin{bmatrix} C \end{bmatrix} \begin{bmatrix} i_{ag} \\ i_{bg} \\ i_{cg} \end{bmatrix}, \quad (8)$$
$$\begin{bmatrix} C \end{bmatrix} = \frac{2}{3} \begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix}$$

The FC voltages can be calculated via the switching state and grid current. However, the dynamic model will be not presented here because of not require their predictive values in the cost function with the proposed method.

TABLE II: The consequences of switching states on the FC voltages

Output level	Grid current	State	Impact on flying capacitor voltages		
L_x	i_{xg}	S_x	u_{cx1}	u_{cx2}	
0	-	0	No impact	No impact	
1	≥ 0	1C 1D	No impact Charge	Discharge Charge	
	< 0	1C 1D	No impact Discharge	Charge Discharge	
2	≥ 0	2C 2D	Discharge Charge	Discharge No impact	
_	< 0	2C 2D	Charge Discharge	Charge No impact	
3	-	3	No impact	No impact	

III. PROPOSED PREDICTIVE DIRECT POWER CONTROL WITH CAPACITOR VOLTAGE BALANCING APPROACH

The 4L-T-type NNPC inverters have two sets of redundant switching vectors that affect the FC voltages concerning the status of the switches and indication of the grid current. There is no influence on FC voltage u_{cx1} with the switching state 1C, whereas, the FC voltage u_{cx2} is charged and discharged in case of $i_{xg} < 0$ and $i_{xg} > 0$, respectively. Meanwhile, the FC voltages u_{cx1} and u_{cx2} undergo charging with positive grid current and discharging with negative grid current when switching state 1D is selected. Similarly, two FC voltages are discharged and charged corresponding to positive and negative currents if selecting the switching status 2C. Regardless of the polarity of the grid current, the switching state 2D does not impact the FC voltage u_{cx2} . Whereas, the FC voltage u_{cx1} is charged with $i_{xg} > 0$ and discharged with $i_{xg} < 0$. In the case of output levels 0 and 3, the FC voltages remain unaffected since the grid current doesn't flow through the FC. Table II illustrates the behavior of FC voltages concerning combination sequences of the switches and grid current for 4L-T-type NNPC inverters.

The voltage deviation of FC is differentiated between the actual value and reference value as:

$$\Delta u_{cxj} = u_{cxj} - \frac{U_{dc}}{3},\tag{9}$$

where u_{cxj} indicates the FC voltage with $j \in \{1, 2\}$.

According to these previous analyses, if $\Delta u_{cxj} > 0$ at the sampling time k, the inverter employs the suitable switching state in the next sampling time to reduce u_{cxj} . On the other hand, the switching vector that charges the capacitor C_{xj} is chosen to balance the FC voltage. In this case, the regulation of voltage balance for the lower capacitor C_{x2} is managed via switching status 1C and 1D. In contrast, the switching status 2C and 2D can be employed to guarantee the balance of FC voltage u_{cx1} [4]. Taking output level 1 as an example, if the voltage deviation of the lower capacitor is negative ($\Delta u_{cx2} < 0$), the switching status 1C is selected with $i_{xg} < 0$, whereas the switching status 1D is chosen with $i_{xg} \geq 0$. When $\Delta u_{cx2} > 0$, the switching status 1D is determined if

 $i_{xg} < 0$; otherwise, the state 1C is applied to the gate of the switches. Besides, if $\Delta ucx1 < 0$, the switching vector 2C is applied to the inverter with the negative current; in other ways, the switching vector 2D is the appropriate solution. When $\Delta u_{cx1} > 0$, switching vector 2D is selected if $i_{xg} > 0$. In the remaining cases, the switching state 2C is the best vector. This paper utilizes a straightforward logic state outlined in Table III to choose the suitable switching state from redundant voltage vectors, ensuring the equilibrium of FC voltages. For instance, when the output level is 1, the switching state 1C is selected with a positive condition ($\Delta u_{cx2} * i_{xg} \ge 0$); otherwise, the switching state 1D is the appropriate switching status.

TABLE III: Simple logic condition of balancing FC voltages

Voltage level	Logic condition	Suitable switching state	
1	$\begin{array}{l} \Delta u_{cx2} * i_{xg} \geq 0 \\ \Delta u_{cx2} * i_{xg} < 0 \end{array}$	1C 1D	
2	$\begin{array}{l} \Delta u_{cx1} * i_{xg} \geq 0 \\ \Delta u_{cx1} * i_{xg} < 0 \end{array}$	2C 2D	

With the assumption of skipping the filter resistance, the grid current is obtained in the $\alpha\beta$ cordinator frame as follows:

$$i_{g\alpha}(k+1) = i_{g\alpha}(k) + \frac{T_s}{L_f} \left(u_{o\alpha}(k) - u_{g\alpha}(k) \right), \quad (10)$$

$$i_{g\beta}(k+1) = i_{g\beta}(k) + \frac{T_s}{L_f} \left(u_{o\beta}(k) - u_{g\beta}(k) \right),$$

where the components of output inverter voltage $u_{o\alpha}(k)$ and $u_{o\beta}(k)$ are given by:

$$\begin{bmatrix} u_{o\alpha}(k) \\ u_{o\beta}(k) \end{bmatrix} = [C] \begin{bmatrix} u_{ao}(k) \\ u_{bo}(k) \\ u_{co}(k) \end{bmatrix} - [C] [N] \begin{bmatrix} u_{ao}(k) \\ u_{bo}(k) \\ u_{co}(k) \end{bmatrix}$$
(11)

Given a little sampling interval T_s and stable grid voltage assumption, the variation in grid power over one sampling period is is derived from equation (7) as:

$$P_{g}(k+1) = P_{g}(k) + \frac{3T_{s}}{2}u_{g\alpha}(k) (i_{g\alpha}(k+1) - i_{g\alpha}(k)) + \frac{3T_{s}}{2}u_{g\beta}(k) (i_{g\beta}(k+1) - i_{g\beta}(k)),$$
(12)
$$Q_{g}(k+1) = Q_{g}(k) + \frac{3T_{s}}{2}u_{g\beta}(k) (i_{g\alpha}(k+1) - i_{g\alpha}(k)) - \frac{3T_{s}}{2}u_{g\alpha}(k) (i_{g\beta}(k+1) - i_{g\beta}(k)).$$

The aim of the control is to follow the grid power reference. Consequently, one can suppose as:

$$P_g(k+1) = P_g^*(k+1), \ Q_g(k+1) = Q_g^*(k+1).$$
 (13)

Combining equations (10), (13) and (12), the required inverter voltage can be calculated as follows:

$$u_{o\alpha}^{*}(k) = u_{g\alpha}(k) + \frac{3L_{f}}{2T_{s}U_{gm}} \left(P_{g}^{*}(k+1) - P_{g}(k)\right) u_{g\alpha}(k) + \frac{3L_{f}}{2T_{s}U_{gm}} \left(Q_{g}^{*}(k+1) - Q_{g}(k)\right) u_{g\beta}(k),$$
(14)

$$u_{o\beta}^{*}(k) = u_{g\beta}(k) + \frac{3L_f}{2T_s U_{gm}} \left(P_g^{*}(k+1) - P_g(k) \right) u_{g\beta}(k) - \frac{3L_f}{2T_s U_{gm}} \left(Q_g^{*}(k+1) - Q_g(k) \right) u_{g\alpha}(k),$$

where $U_{gm} = v_{g\alpha}^2 + v_{g\beta}^2$.

The conventional FCS-MPC uses 216 possible control inputs of the 4L-T-type NNPC inverters to optimize the cost function for achieve the most suitable switching combination. Therefore, this causes a heavy computation burden, leading to a long sampling time or a powerful processor. In order to decrease the great computation, numerous approaches are offered in [9], [10]. Theses methods combined the sector location of desired inverter voltage vector and the FCS-MPC to reduce the number of control switching state for optimization loop. In this case, the possible inverter voltage vector of the 4L-T-type NNPC is decreased from 64 to 20 as shown in Figure 2. Nevertheless, the cost function is evaluated with 72 feasible switching status considering the various influences of redundant switching vector on the balance of FC voltages. Besides, the selection of the optimal weighting factor is a time-consuming effort in an actual system. To address aforementioned issues, a proposed method is presented in our paper that not only reduces the heavy computation burden but also guarantees the self-balance of FC voltages without a weighting factor. The control strategy has two stages. In the first stage, the sector location of the required inverter voltage is determined according to predictive and necessary grid powers and voltage. Then, the best inverter voltage vector is achieved from the optimization loop of the cost function. In the next stage, the optimal switching state is accomplished based on the previous simple logic condition as mentioned in Table III to balance the FC voltages. For instance, if the best inverter voltage level is 1, the switching state 1C is selected in case of $\Delta u_{cx2} * i_{xg} \ge 0$ while the switching state 1D is chosen in the reverse condition. Similarly, we can select the appropriate switching state 2C and 2D respectively for output voltage level 2. In this sense, the proposed technique uses only one switching state for each redundant voltage vector, resulting in a reduction of the number of control inputs to 20 for the optimization problem. Therefore, our control method provides an alternative solution to facilitate computational efforts and perform self-maintaining of FC voltages without weighting factor selection. The proposed strategy is summarized as follows:

- Step 1: Measure $i_g(k)$, $u_g(k)$, $U_{dc}(k)$; Read $u_{cx}^*(k)$, $P_g^*(k)$ and $Q_g^*(k)$.

- Step 2: Calculate the deviation of FC voltage utilizing (9).

- Step 3: Compute the components of desired inverter voltage $v_{o\alpha}^*(k)$, $v_{o\beta}^*(k)$ using(14).

- Step 4: Specify the sector place of inverter voltage.

- Step 5: Initialize the cost function and best inverter voltage.

- *Step 6*: Enumerate the cost function and select the most suitable inverter voltage among the 20 possible combinations of the predefined sector:

+ Predict grid current $i_a(k+1)$ via (6)

+ Predict the grid power: $P_g(k+1)$ and $Q_g(k+1)$ using (7)

+ Enumerate the cost function
$$g(u_k) = \|P_g^*(k+1) - P_g(k+1)\|^2 + \|Q_g^*(k+1) - Q_g(k+1)\|^2$$

+ Select the optimal inverter voltage

- *Step 7*: Determine the suitable switching state for inverter voltage levels 1 and 2 through Table III.

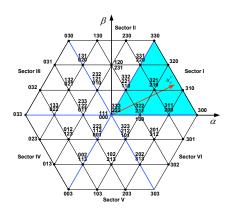


Fig. 2: Sector location of voltage vectors produced by the 4L-T-type NNPC inverter.

IV. SIMULATION RESULTS

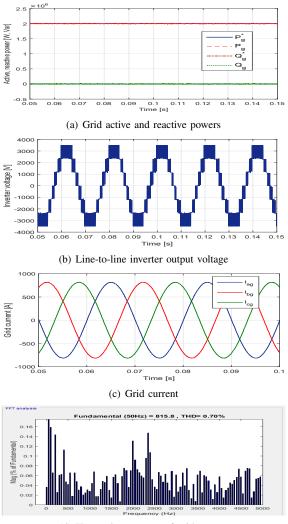
Simulation examinations were carried out using Matlab/Simulink software to verify the proposed method's effectiveness. The parameters of the system studied are presented in Table IV. The control performance of the suggested approach is analyzed in both transient-state and steady-state conditions.

TABLE IV: Simulation investigation specifications.

Parameters	Value
Power rating	2 MVA
Line-to-line grid voltage	2 kV
Grid frequency	50 Hz
Filter resistance	$40 \text{ m}\Omega$
Filter inductance	3 mH
DC-link voltage	3500 V
Flying capacitor	$2000 \ \mu F$
Sampling period	50 μs

A. Steady-state analysis

Fig. 3(a) demonstrates the steady-state of the grid active power ($P_g = 2$ MW) with unity power factor ($Q_g = 0$) for the proposed strategy. As highlighted in this figure, the suggested approach achieves high control performance with small steady



(d) Harmonic spectrum of grid current

Fig. 3: Stable performance of the offered approach under the condition of $P_q = 2$ MW and a power factor of 1.

errors of power ripples. Figure 3(c) clearly illustrates that the proposed technique accomplishes the sinusoidal three-phase grid current. Fig. 3(b) also depicts the square pattern of the inverter output voltage between the line-to-line. The stable performance of the grid current is assessed using a Fast Fourier Transform from the Powergui toolbox. Fig. 3(d) indicates that the total harmonic distortion (THD) of the current is 0.7% that satisfies the requirement of the IEEE 519-2014 standard.

B. Dynamic examination

To demonstrate the efficiency of the control approach, a comparison investigation between the developed method and the traditional FCS-MPC [1], [3] is introduced in Fig. 4. At time t = 0.1 s, the active power reference is altered from 0.5 to 2 MW, whereas maintaining the reactive power at zero. It is clear that the suggested control algorithm has satisfactory tracking behavior with a fast transient response and minimal overshoot similar to the conventional FCS-MPC.

Figure 4(b) illustrates that both control methods reach a steady-state condition within 3.7 ms in terms of their active power response. The related behaviors of the grid current for two control strategies are displayed in Figs. 4(c) and 4(d). The achieved results confirm that the proposed control algorithm has high tracking quality with low stable error, fast transient response of grid power and low THD of the current. Our contribution's significance is in reducing computational burden and eliminating cumbersome procedures in the tuning process of a weighting factor. Moreover, the tic-toc toolbox is used to measure the calculation time of the control algorithm. The new approach reduces the average computation time by 50% in comparison with the traditional method. Furthermore, the traditional strategy takes longer to compute than the sampling time (50 μ s), which is a restriction of this method. Therefore, our technique suggests an additional solution for implementing the FCS-MPC algorithm to multilevel inverters using an affordable processor and a brief sampling interval. The control performance of six flying capacitor voltages is illustrated in Fig. 4(e). It is worthwhile noting that the flying capacitor voltage balancing is assured at $V_{dc}/3$ even though a variation occurred of active power.

To demonstrate the efficacy of the developed balancing approach, the investigated system is studied under three different unconventional operations. First, the voltages of FC are initialized at $V_{dc}/2$). After, both voltages of FC are adjusted to zero and $V_{dc}/2$, respectively. Finally, further examination was conducted with $u_{ca1} = V_{dc}/2$ and $u_{ca2} = 0$. It is apparent from Fig. 5 that the FC voltages can quickly reach the desired value despite the initial voltage across the capacitor.

V. CONCLUSIONS

This paper presents an advanced FCS-MPC approach designed to control power flow directly between the grid and 4L-T-type NNPC inverters. The key advantages of our study are to significantly decrease the high computational cost and guarantee the balance of FC voltages by utilizing the achievable switching status for a duplicative voltage vector, leading to eliminating the bulky procedures in the tuning process of a weighting factor. The proposed technique not only has equivalent control performance compared to the conventional method in dynamic and stable conditions, including settling time, power errors, and the THD of the grid current, but it is also less time-consuming. Therefore, our strategy provides an alternative resolution for applying the FCS-MPC approach with an inexpensive processor and a brief sampling interval.

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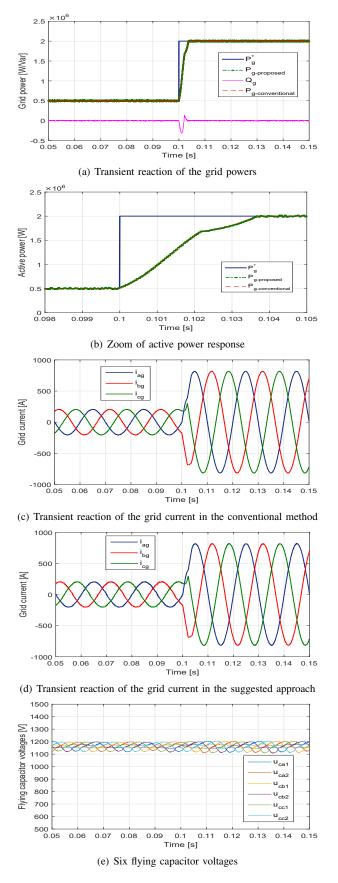


Fig. 4: The response during a sudden change in active power.

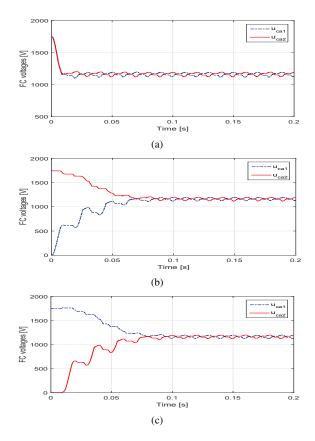


Fig. 5: Behavior of capacitor voltages for u_{ca1} and u_{ca2} under varying initial voltage settings: (a) $u_{ca1} = 0$ and $u_{ca2} = U_{dc}/2$. (b) $u_{ca1} = u_{ca2} = U_{dc}/2$. (c) $u_{ca1} = U_{dc}/2$ and $u_{ca2} = 0$.

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