Enhanced Model Predictive Control Using Modified Space Vector Modulation for Grid-Connected 3L-NPC Inverters

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***Abstract*— This paper presents a power control strategy for a grid-connected three-level neutral-point-clamped inverter. The proposed approach integrates Model Predictive Control (MPC) with a modified Space Vector Modulation (SVM) scheme. The control structure comprises an inner current control loop and an outer DC-link voltage control loop to regulate both active and reactive power. To address the neutral-point voltage imbalance issue, a modified SVM method is developed by adaptively adjusting the dwell times of voltage vectors. This approach effectively balances the capacitor voltages, mitigates voltage fluctuations, and reduces current harmonic distortion. Simulation results in Matlab/Simulink verify that the active and reactive powers accurately track their reference values, achieving minimal steady-state error and fast dynamic response. In addition, the DC-link voltage remains stable, and the capacitor voltages are well balanced even under the application of medium voltage vectors. Furthermore, compared with the conventional finite control set MPC (FCS-MPC), the proposed method achieves superior performance in terms of lower total harmonic distortion of the grid current, owing to its fixed switching frequency, as well as reduced neutral-point voltage ripple.**

Keywords – Grid-side converter; power control; three-level neutral-point clamped inverter; space vector modulation; neutral-point voltage balancing; finite control set model predictive control.

I. INTRODUCTION

Among grid-side converter topologies, the three-level neutral-point-clamped (3L-NPC) inverter is widely adopted in industrial drives and renewable energy applications due to its reduced harmonic distortion, lower switching device voltage stress, and increased power capacity compared to conventional two-level inverters [1]. However, the inherent DC-link capacitor voltage imbalance remains a critical challenge, as it degrades power quality and may lead to device failure [2]–[5]. Although several solutions, including virtual vector methods [6] and conventional finite control set model predictive control (FCS-MPC) [6-9], have been proposed, they often exhibit drawbacks such as high computational complexity, increased switching losses, or variable switching frequencies, which complicate filter design.

To address these challenges, this paper proposes an enhanced control scheme that combines a finite control set model predictive control (FCS-MPC) structure with an improved space vector modulation (SVM) strategy. The control architecture incorporates an inner current loop and an outer DC-link voltage loop to ensure accurate active and reactive power regulation. Meanwhile, the SVM block dynamically adjusts the dwell times of redundant voltage vectors using a regulation factor (P) to maintain neutral-point voltage balance. This approach further optimizes the switching sequence based on the polarity of the capacitor voltages and the phase currents. Simulation results obtained in Matlab/Simulink demonstrate that, compared with conventional FCS-MPC, the proposed method significantly reduces the total harmonic distortion of the grid current, achieves a fixed switching frequency, and ensures robust neutral-point voltage stability under both steady-state and dynamic operating conditions.

The remainder of this paper is organized as follows. Section II presents the control structure of the grid-side converter (GSC). Section III outlines the proposed enhancements to the SVM modulation scheme. Section IV provides simulation results and analysis. Finally, Section V concludes the paper and outlines future research directions.

II. CONTROL SCHEME FOR THE GRID-SIDE CONVERTER

A. Control Structure Design

To design the control structure for the grid-side converter (GSC), the system is modeled in the synchronous dq reference frame using the Park–Clarke transformation. The voltage and current dynamics of the grid-connected 3L-NPC inverter can therefore be expressed in the dq reference frame as follows [10]:

$$u_{gd} = -L_f \frac{di_{gd}}{dt} - R_f i_{gd} + u_{inv,d} + \omega L_f i_{gq} \quad (1)$$

$$u_{gq} = -L_f \frac{di_{gq}}{dt} - R_f i_{gq} + u_{inv,q} - \omega L_f i_{gd} \quad (2)$$

$$C_{dc} \frac{dU_{dc}}{dt} = i_{load} - \frac{3}{2} \frac{V_s}{U_{dc}} i_{gd} \quad (3)$$

where u_{gd}, i_{gd} and u_{gq}, i_{gq} denote the grid voltage and current components along the d- and q-axes, respectively; ω represents the angular frequency of the grid voltage.

$u_{inv,d}, u_{inv,q}$ are the output voltages of the GSC in the synchronous *dq* reference frame. In (3), C_{dc}, U_{dc}, and i_{load} denote the DC-link capacitance, DC-link voltage, and DC-side load current, respectively.

The control structure of the GSC consists of an inner current control loop to regulate i_{gd} and i_{gq}, and an outer DC-link voltage control loop to maintain the stability of U_{dc} (Figure 1). In this configuration, the *d*-axis current component is responsible for controlling the active power and regulating the DC-link voltage, whereas the *q*-axis current component governs the reactive power.

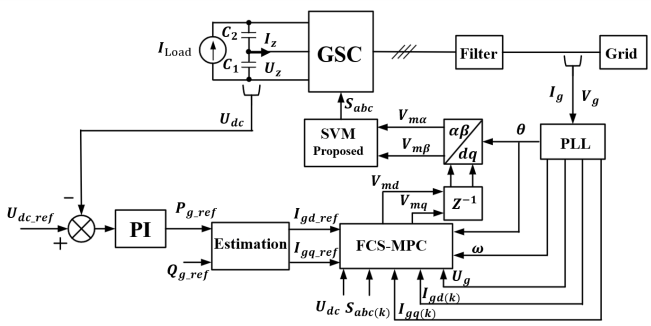


Figure 1. Control structure of the GCS.

B. MPC Controller Design for a Current Loop Circuit

The grid current dynamics can be derived from (1) and (2) as follows [7]:

$$\begin{aligned}\frac{di_{gd}}{dt} &= \frac{1}{L_f}\left(u_{inv,d} - R_f i_{gd} - u_{gd} + \omega L_f i_{gq}\right)\\ \frac{di_{gq}}{dt} &= \frac{1}{L_f}\left(u_{inv,q} - R_f i_{gq} - u_{gq} - \omega L_f i_{gd}\right)\end{aligned} \tag{4}$$

Since the system is aligned with the grid voltage, the grid voltage components can be expressed as: $u_{gq} = 0, u_{gd} = U_g$, where U_g is the amplitude of the grid voltage determined by the phase-locked loop (PLL). In addition, the inverter output voltage in the *dq* reference frame can be estimated from the switching state as:

$$\begin{aligned}u_{inv,d} &= \frac{U_{dc}}{6}\left[\left(2S_a - S_b - S_c\right)\cos\theta + \sqrt{3}\left(S_b - S_c\right)\sin\theta\right]\\ u_{inv,q} &= \frac{U_{dc}}{6}\left[\sqrt{3}\left(S_b - S_c\right)\cos\theta - \sqrt{3}\left(2S_a - S_b - S_c\right)\sin\theta\right]\end{aligned} \tag{5}$$

where θ is the grid voltage phase angle.

Using (4) and a sampling time T_s, the discrete-time prediction of the grid currents can be obtained via the first-order forward Euler approximation as follows:

$$\begin{aligned}i_{gd}(k+1) &= \frac{T_s}{L_f}\left(u_{inv,d}(k) - U_g\right) + \left(1 - \frac{R_f T_s}{L_f}\right) i_{gd}(k) + \omega T_s i_{gq}(k)\\ i_{gq}(k+1) &= \frac{T_s}{L_f} u_{inv,q}(k) + \left(1 - \frac{R_f T_s}{L_f}\right) i_{gq}(k) - \omega T_s i_{gd}(k)\end{aligned} \tag{6}$$

where $u_{inv,d}(k)$ and $u_{inv,q}(k)$ can be determined from the previous control input u_k and U_{dc} using (5). Similarly, the reference inverter output voltage components are obtained as:

$$\begin{aligned}u^*_{inv,d}(k+1) &= \frac{L_f}{T_s} i^*_{gd}(k+2) + \left(R_f - \frac{L_f}{T_s}\right) i_{gd}(k+1) + U_g - \omega L_f i_{gq}(k+1)\\ u^*_{inv,q}(k+1) &= \frac{L_f}{T_s} i^*_{gq}(k+2) + \left(R_f - \frac{L_f}{T_s}\right) i_{gq}(k+1) + \omega L_f i_{gd}(k+1)\end{aligned} \tag{7}$$

where the predictive reference current is estimated using second-order Lagrange extrapolation as follows:

$$\begin{aligned}i^*_{gd}(k+2) &= 6i^*_{gd}(k) - 8i^*_{gd}(k-1) + 3i^*_{gd}(k-2)\\ i^*_{gq}(k+2) &= 6i^*_{gq}(k) - 8i^*_{gq}(k-1) + 3i^*_{gq}(k-2)\end{aligned} \tag{8}$$

Based on the active and reactive power references, the grid current references are determined as follows:

$$i^*_{gd}(k) = \frac{2}{3}\frac{P_g^*}{U_g},\ i^*_{gq}(k) = -\frac{2}{3}\frac{Q_g^*}{U_g} \tag{9}$$

In this paper, the neutral-point voltage balance is guaranteed by employing the proposed SVM, which is presented in the next section. Finally, the objective of the proposed predictive control is achieved by evaluating an appropriate cost function for all possible switching states according to the following steps:

- *Step 1*: Measure $i_g(k)$, $u_g(k)$ and $U_{dc}(k)$; read the reference values $U^*_{dc}(k)$ and $Q^*_g(k)$
- *Step 2*: Estimate the grid currents $i_{gd}(k+1)$ and $i_{gq}(k+1)$ using (6)
- *Step 3*: Compute the reference grid currents $i^*_{gd}(k)$ and $i^*_{gq}(k)$ from (9), and the inverter output voltage references $u^*_{inv,d}(k+1)$ and $u^*_{inv,q}(k+1)$ from (7) and (8)
- *Step 4*: Calculate the inverter output voltage components for all feasible switching states $u_{inv,d}(k+1)$ and $u_{inv,q}(k+1)$ based on (5);
- *Step 5*: Compute the number of switching transitions

$$n_c = \sum_{x=a,b,c} \left\| S_x(k+1) - S_x(k) \right\|^2$$

- *Step 6*: Evaluate the cost function to select the optimal inverter voltage, which is then applied to the SVM by minimizing the following cost function [7-9]:

$$\begin{aligned}g_{grid}(u_k) = &\left\| u^*_{inv,d}(k+1) - u_{inv,dn}(k+1) \right\|^2 + \left\| u^*_{inv,q}(k+1) - u_{inv,qn}(k+1) \right\|^2\\ &+ \lambda_n n_c,\end{aligned} \tag{10}$$

$$u_{opt} = \arg\left\{\min(g_{grid}(u_k))\right\}, n = 1,...,27$$

C. *DC Voltage Loop Controller Design*

The DC-link voltage control loop plays a crucial role in maintaining the stability of the DC-link voltage while generating the reference current i_{gd}^{*} for the inner current control loop. The power balance equation between the DC and AC sides is given as follows [10]:

$$P_{load} - P_g = \frac{1}{2} C_{dc} \frac{dv_{dc}^2}{dt} \tag{11}$$

Based on the power voltage relationship, a proportional-integral (PI) controller is employed for the DC-link voltage loop. As the voltage loop operates as the outer loop of the cascaded control structure, its time constant is deliberately chosen to be larger than that of the inner current loop to guarantee system stability. By choosing v_{dc}^2 as the control variable, the system dynamics are formulated as follows:

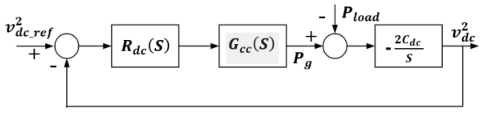


Figure 2. DC-link voltage control loop diagram.

The closed-loop transfer function of the inner current control loop, after controller synthesis, can be expressed as:

$$G_{cc}(s) = \frac{1}{1 + sT_{dc1}} \tag{12}$$

The controller is designed in the form: $R_{dc}(s) = K_{pv} \frac{1 + sT_{dc1}}{1 + sT_{dc2}}$ (13)

The closed-loop transfer function of the voltage control loop is given by:

$$G_v(s) = \frac{2K_{pv}}{2K_{pv} + T_{dc2} s^2 C_{dc} + sC_{dc}} = \frac{\omega_n^2}{s^2 + 2\omega_n \xi s + \omega_n^2} \tag{14}$$

where ω_n is the natural frequency and ξ is the damping ratio of the system. Accordingly, the parameters of the voltage controller are determined as follows:

$$T_{dc2} = \frac{1}{2\omega_n \varepsilon}, K_{pv} = \frac{C_{dc}\omega_n}{4\varepsilon} \tag{15}$$

III. Proposed Modified Three-Level Space Vector Modulation Method

A. *Space Vector Diagram*

Among the 27 switching states of the 3L-NPC inverter, 19 unique voltage vectors are obtained to form the space vector diagram. These vectors are distributed into six main sectors, each further divided into four subregions, as illustrated in Figure 3. Based on the magnitude of the voltage vectors, they can be classified into four groups: large vectors (PNN, PPN, NPN, NPP, NNP, PNP), medium vectors (PON, OPN, NPO, NOP, ONP, PNO), small vectors (ONN, POO, OON, PPO, OPN, NON, OPP, NOO, OOP, NNO, POP, ONO), and zero vectors (PPP, NNN, OOO).

The large vectors and zero vectors have no impact on the neutral-point voltage (u_z), whereas the small and medium vectors contribute to neutral-point voltage imbalance in the 3L-NPC inverter. In particular, there exist two redundant switching state pairs of the small vectors that produce the same output voltage but have opposite effects on the neutral-point voltage. For instance, negative vectors such as POO increase the neutral-point voltage, while positive vectors such as ONN decrease u_z .

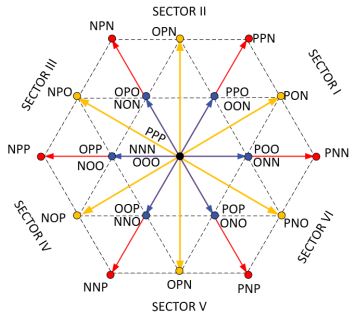


Figure 3. Space vector diagram of the 3L-NPC inverter.

B. *Proposed Cotrol Algorithm*

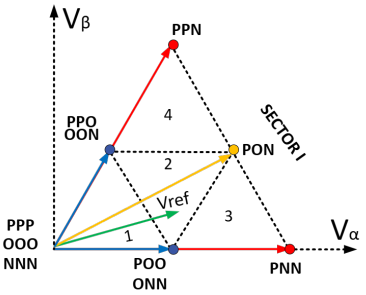


Figure 4. Reference vector located in region 2 of sector I.

$$\begin{cases} T_s \vec{V}_{ref} = T_a \vec{V}_1 + T_b \vec{V}_7 + T_c \vec{V}_2 \\ T_s = T_a + T_b + T_c \end{cases} \tag{16}$$

The analysis of Sector I - Region 2 in the space vector diagram is illustrated in Figure 4. In this region, the reference vector is synthesized using three nearest vectors, including one medium vector (PON) and two small vectors. To ensure neutral-point voltage balancing, the dwell times of the small vectors are properly adjusted, either increased or decreased, according to the algorithm shown in Figure 5. Let i_a denote the phase current associated with a redundant vector pair (POO and ONN). The neutral current corresponding to the switching state

POO is opposite to i_a ($i_z = -i_a$), whereas for ONN, it is in the same direction as i_a ($i_z = i_a$). When $\Delta v = v_{c2} - v_{c1} > 0$, if the corresponding phase current $i_a > 0$, then $sign(\Delta v)sign(i_a) > 0$. In this case, the dwell time of vector POO which contributes to increasing the neutral-point voltage ($i_z < 0$) is increased, while the dwell time of vector ONN which decreases the neutral-point voltage ($i_z > 0$) is reduced. Consequently, v_{c2} decreases and v_{c1} increases, leading to a reduction in Δv. Conversely, if the phase current is negative, then $sign(\Delta v)sign(i_a) < 0$. In this situation, the dwell time of vector POO is reduced, while that of vector ONN is increased. As a result, v_{c2} decreases and v_{c1} increases, which also reduces Δv. For the case $\Delta v < 0$, the procedure is reversed. A similar strategy is applied to the other phase currents and their corresponding redundant vector pairs.

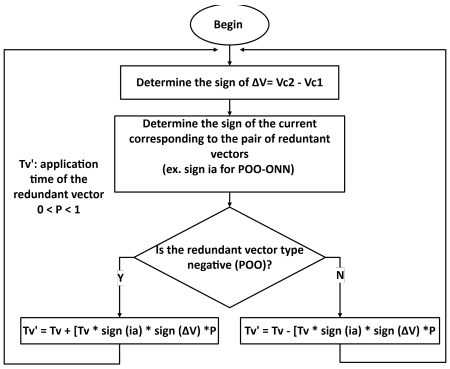


Figure 5. Algorithm for dwell time calculation.

With:
$$\begin{cases} \lambda_1 = \frac{T_a}{4} * \mathrm{sgn}(i_a) * \mathrm{sgn}(\Delta v) * P \\ \lambda_2 = \frac{T_c}{4} * \mathrm{sgn}(i_c) * \mathrm{sgn}(\Delta v) * P \end{cases} \quad (17)$$

C. Dwell Time Calculation of Space Vectors

To minimize switching transitions, reduce switching losses, and extend the lifetime of power devices, the switching states are arranged such that consecutive vectors differ by only one switching action. A symmetrical switching sequence is then employed, with dwell times assigned according to the position of the reference vector. This approach enables a balanced switching frequency distribution among inverter legs and reduces harmonic distortion in the output voltage.

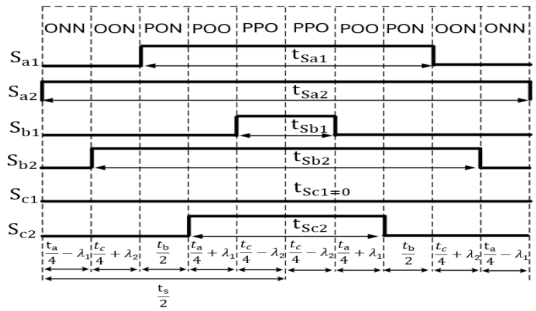


Figure 6. Switching sequence and specific dwell times for each state in region 2 of sector I.

Based on the dwell time distribution of the symmetrical switching sequence shown in Figure 6, the switching instants for each inverter leg (a, b, and c) over a complete switching period can be derived as follows:

$$\begin{cases} t_{sa1} = \frac{T_a}{2} + \frac{T_c}{2} + T_b + 2(\lambda_1 - \lambda_2) \\ t_{sa2} = T_s \\ t_{sb1} = \frac{T_c}{2} - 2\lambda_2 \\ t_{sb2} = T_s - \frac{T_a}{2} + 2\lambda_1 \\ t_{sc1} = 0 \\ t_{sc2} = \frac{T_a}{2} + \frac{T_c}{2} + 2(\lambda_1 - \lambda_2) \end{cases} \quad (18)$$

IV. Simulation Validation

To verify the control performance of the proposed scheme for the grid-tied 3L-NPC inverter, simulations were conducted in the Matlab/Simulink environment using the SimPowerSystems toolbox. The system parameters are listed in Table 1.

To evaluate the performance, we use the mean absolute percentage error (MAPE) which can be expressed as follows:

$$MAPE = \frac{1}{n}\sum_{i=1}^{n}\left|\frac{y_i^* - y_i}{y_i^*}\right| \quad (19)$$

where y_i^* is the reference vector and y_i is the vector measured.

TABLE I. Simulation Parameters of the System.

Parameters	Values
Rated Power	660 (kW)
DC-Link Voltage	1150 (V)
Grid Voltage	380 (V)
Grid Frequency	50 (Hz)
DC-Side Capacitance	C = 20 (mF)
Filter Inductance	L = 0,5 (mH)
Filter Resistance	R = 1,8 (mΩ)
Modulator Sampling Frequency	10 (kHz)

A. Steady-State Evaluation

The steady-state simulation results are presented in Figures 7–9. As shown in Figure 7, the grid current exhibits a smooth sinusoidal waveform with a very low total harmonic distortion (THD) of 0.87%, as analyzed using the built-in FFT tool in Simulink. The desired grid active power is maintained at 660 kW with a unity power factor. As observed in Figure 8, the output power closely follows the reference value. Furthermore, the neutral-point voltage remains well balanced, exhibiting only slight oscillations around zero, as illustrated in Figure 9.

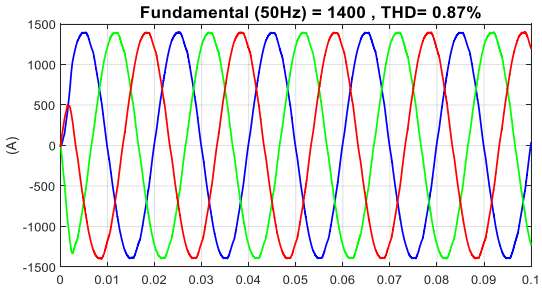


Figure 7. Three-phase grid currents and THD of the phase current.

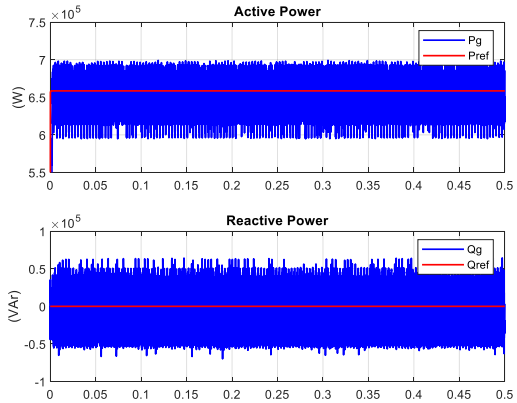


Figure 8. Grid active and reactive power under steady-state conditions.

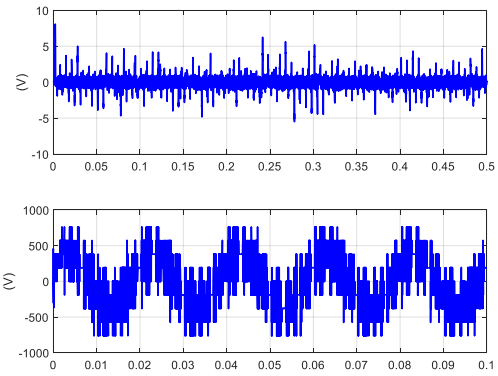
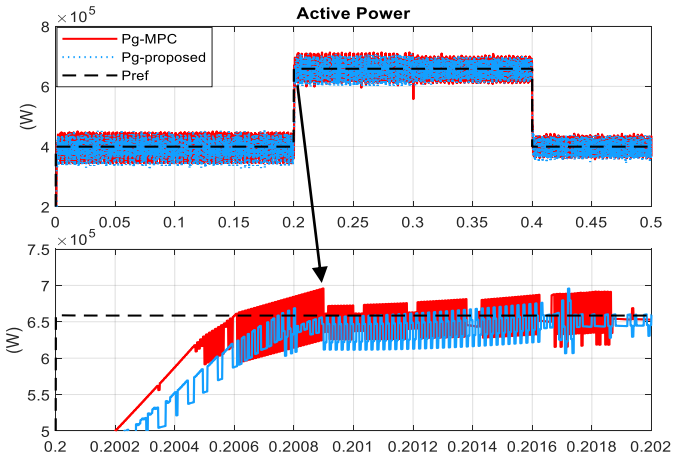


Figure 9. Neutral point voltage and inverter output voltage.

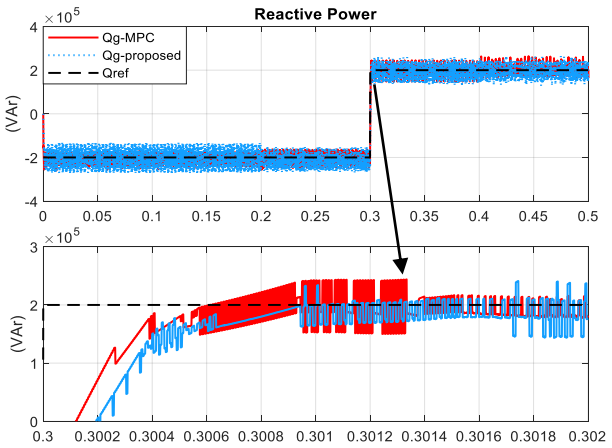
B. Dynamic Response Evaluation

To validate the effectiveness and feasibility of the proposed method, a comparative study is carried out between the conventional FCS-MPC [9] and the proposed FCS-MPC with SVM under identical operating conditions.

At t = 0.2 s, the active power is increased from 400 kW to 660 kW and then reduced back to 400 kW at t = 0.4 s, as illustrated in Figure 10(a). The simulation results demonstrate that the proposed method achieves superior that the proposed method achieves superior performance, characterized by a fast dynamic response, reduced ripple, and a significantly lower



a)



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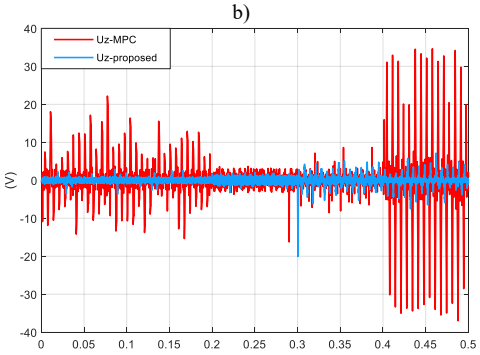

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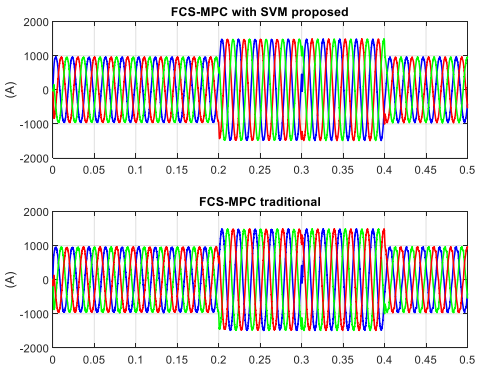
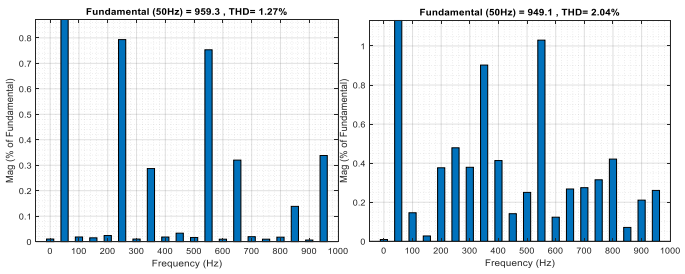


d)



e)

Figure 10. Comparison of simulation results between the proposed and conventional methods in dynamic response mode: a) grid's active powers, b) grid's reactive powers , c) neutral-point voltages, d) grid currents, e) FFT analysis of currents.

overshoot of only 1.5%, compared to 6.06% for the conventional method. Notably, at t = 0.4 s, the neutral-point voltage in the conventional method becomes severely unbalanced, as shown in Figure 10(c), which leads to a reactive power response with large overshoot and pronounced oscillations. In contrast, the proposed method maintains better stability under the same conditions. The grid current remains nearly sinusoidal in both cases; however, the THD is reduced from 2.04% in the conventional method to 1.27% with the proposed method, as illustrated in Figure 10(d). Furthermore, the FFT analysis in Figure 10(e) shows that the proposed method effectively suppresses most even-order harmonic components by employing the SVM technique to ensure a fixed switching frequency. Additionally, the MAPE of the active power is reduced from 3.77% to 2.45% when using the proposed approach, further confirming its improved accuracy over the conventional FCS-MPC method. The results indicate that the proposed method outperforms the conventional approach by providing faster response, improved current quality, better neutral-point voltage balance, enhanced DC-link stability, and reduced harmonic distortion, which simplifies the grid filter design. Table 2 provides a comparative analysis of the two control methods, demonstrating the superior performance of the proposed strategy across various operating scenarios.

TABLE II. A COMPARATIVE EVALUATION OF THE TWO CONTROL APPROACHES.

Criteria	**Proposed method**	**Conventional method**
MAPE of P_g (%)	2.45	3.77
Settling time (ms)	0.9	0.92
Transient time (ms)	0.6	0.62
THD of current (%)	1.27	2.04
Neutral-point voltage deviation (%)	0.435	3.04
Overshoot (%)	1.5	6.06

V. CONCLUSIONS

This paper presents a control strategy for grid-connected 3L-NPC inverters by integrating FCS-MPC with an improved SVM scheme to achieve effective neutral-point voltage balancing. The proposed method reduces the neutral-point voltage deviation to 0.435%, compared to up to 3.04% in conventional FCS-MPC, highlighting its superior balancing performance. In addition, the improved SVM ensures a fixed switching frequency, reduces current harmonics, and enhances the regulation of active and reactive power control with minimal ripple. The approach also achieves faster dynamic response with reduced overshoot. Overall, the proposed strategy is simple, practical, and well-suited for renewable energy systems and grid-connected converters. Future work will focus on extending the method to advanced multilevel topologies, such as four-level NPC, T-type, and ANPC inverters, and validating its performance through real-time DSP/FPGA implementation.

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